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09/757,537	01/11/2001	Hiroshi Tanaka	21.1989	8110

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EXAMINER	
FERRIS, DERRICK W	

ART UNIT	PAPER NUMBER
2663	

DATE MAILED: 09/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/757,537	Applicant(s) TANAKA, HIROSHI	
	Examiner Derrick W. Ferris	Art Unit 2663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 January 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 14-16* is/are rejected.

7)☒ Claim(s) *13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 January 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. **Claims 1, 3-6, 8, 9, 12, and 14-16** are rejected under 35 U.S.C. 102(e) as being anticipated by UK Patent Application GB 2 322 744 A to *Sasaki et al.* ("*Sasaki*").

As to **claim 1**, see figure 2 where the state of the switches is taught by switches 512-515. In particular, figure 12 teaches that if one of said switches is turned on (step 44) the state is "read in" such that a loop back test execution module 46 is launched or set (step 46) which further teaches a step of determining whether a read state of said switches satisfies a predetermined state (i.e., the predetermined state being executing the loop back test). Finally, notifying the results of said determination, is taught by adjusting the LEDs 501-507 on the front panel, see e.g., pages 40-43.

As to **claim 3**, see similar rejection to claim 1 where the operational test is the loopback test.

As to **claim 4**, different types of loopback tests are performed based on the switch selected, see e.g., pages 40-43.

As to **claim 5**, see similar rejection to claim 1 where the operating condition is stored in a loop back test execution module in ROM or a recording medium and setting up operating conditions read from said recording medium to components of said transmission device are taught as part of performing the loopback test. Finally the test submitted is the actual loopback test performed in a "test mode".

As to **claim 6**, see similar rejection to claim 1 where the setting switches are e.g., switches 511-516 or the switches for the hardware setting terminal, the unit reading the content stored in a recording medium is MPU 2 with the recording medium being RAM 3 and ROM 4 and a unit assigning operating conditions read from the recording medium to said setting switch is MPU2.

As to **claim 8**, see similar rejection to claim 6 where the different tests are the different loop tests.

As to **claim 9**, shown in figure 2 RAM3 and ROM 4 are internal to the device.

As to **claim 12**, see similar rejection to claim 1 where an external medium control unit is MPX 6 or modulation/demodulation 7 and RAM 2 or ROM 4 are considered external to the controller.

As to **claim 14**, see similar rejection to claim 1.

As to **claim 15**, the indicator is the operation display 501-506.

As to **claim 16**, the first switch module is switch 512, the second switch module is switch 513 and the device control unit is the MPU 2.

3. **Claims 1, 3-11, 14 and 16** are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,708,301 B1 *Ohta et al.* ("*Ohta*").

As to **claim 1**, see figure 1 where the device is 1. The plurality of switches are shown as test data output circuits 12 and 22 (i.e., note e.g., that the switches are set in figure 10). The decision Results Output Circuits 16, 26 and 36 determine whether a read state of said switches satisfies a predetermined state, see e.g., figure 2. Finally, the "go/no go" determination step is used to notify results of said determination.

As to **claim 3**, see similar rejection to claim 1 where determining which of said switches is turned on is shown e.g., in figure 2. Operational conditions are set as zeros or ones and tested based on a predetermined pattern, see e.g., column 13, line 50 – column 14, lines 45 in relation to figure 4. For example, one type of operational test might be to test for a short circuit fault, see e.g., column 17, lines 33-40.

As to **claim 4**, different tests are performed, see e.g., figure 5 which uses different bit patterns.

As to **claim 5**, see similar rejection to claim 3 where the operating conditions are stored (i.e., from a recording medium) as shown in figure 10. From the operating conditions certain tests are performed such as testing for a short circuit.

As to **claim 6**, the setting switch is shown as one of the bits for the test data output circuit 12 or 22. A unit read content is shown as part of the Decision Output Circuit 16, 26, or 36. A unit assigning operating conditions is also part of the Decision Output Circuit 16, 26, or 36 which tests e.g., for short circuits.

As to **claim 7**, see similar rejection to claim 1 where the latch 121 in figure 10 may or may not be set constituting either a recording medium or no recording medium.

As to **claim 8**, a plurality of switches are the test data output circuits 12 or 22 which have multiple values, see e.g., figure 5. The device controller and recording medium is the Decision Output Circuit 16, 26, or 36.

As to **claim 9**, the recording medium is internal to the Decision Output Circuit 16, 26, or 36 and thus internal to the device.

As to **claim 10**, a plurality of first switches are the input to the test mode decoder 4 where the test mode decoder 4 is a device controller shown in figure 1. A plurality of second switches are the test data output circuits 12 and 22 shown in figure 1 and in more detail in e.g., in figure 10. The recording medium is the latch of the switches as shown in figure 10 which contains on-off status information. The device controller or test mode decoder setups the test to be preformed or determines which of the switches is to be selected. Operating conditions are predetermined based on the status of the second switches or test data output such as testing for short circuits, see e.g., column 17, lines 33-40.

As to **claim 11**, different from claim 9, the detector output circuit is separate from the test data circuit and thus is also external.

As to **claim 14**, see similar rejection to claims 1 and 8. The indicator is taught as the output of the test result output circuit.

As to **claim 16**, a first switch module is taught as test data output circuit 12, a second switch module is taught as test data output circuit 22, and a device control unit is taught as part of test mode decoder 4.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 2 and 15** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,708,301 B1 *Ohta et al.* ("*Ohta*") in view of UK Patent Application GB 2 322 744 A to *Sasaki et al.* ("*Sasaki*").

In making a proper obviousness rejection under MPEP 706.02(j), the examiner will address the following four steps:

a) *the relevant teachings of the prior art relied upon, preferably with reference to the relevant column or page number(s) and line numbers where appropriate;*
b) *the difference of differences in the claim(s) over the applied cited references;*
c) *the proposed modification of the applied reference(s) necessary to arrive at the claimed subject matter; and*
d) *an explanation why one skilled in the art at the time of the invention was made would have been motivated to make the proposed modification.*

As such to **claim 2**, for step (a) *Ohta* discloses the limitations in the parent claim.

For step (b) *Ohta* is silent or deficient to the further limitation display the result by turning off the display when said read state of said switches corresponds to a predetermined value. In particular, *Ohta* teaches generating a go,no-go signal based on the result which may be used as an external monitoring, see e.g., column 14, lines 31-45 but does not specifically mention using a LED as a go,no-go signal.

Sasaki teaches the further recited limitation above at e.g., figures 1 and 2. In particular, *Sasaki* teaches turning off a LED if there are no errors (i.e., a go signal).

For step (c), the proposed modification of the above-applied reference(s) necessary to arrive at the claimed subject matter would be to modify *Ohta* by clarifying that a LED is used to inform the user of a go,no-go siganl.

In order to establish a prima facie case of obviousness for step (d), three basic criteria must be met. The three criteria according to MPEP 706.02(j) are as follows:

First there must be some suggestion or modification, either in the reference(s) themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine the reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

As such, for step (d) examiner notes that it would have been obvious to one skilled in the art prior to applicant's invention to include the further limitation display the result by turning off the display when said read state of said switches corresponds to a predetermined value. In particular, the motivation for modifying the reference or to combine the reference teachings would be to notify the operator of the state of the device such by using a LED. In particular, *Sasaki* cures the above-cited deficiency by providing a motivation found at e.g., figure 1 and figure 4. Second, there would be a reasonable expectation of success since *Sasaki* teaches testing the internal hardware where the hardware may be a computer chip as taught by *Ohta*. Furthermore the no-go signal taught by *Ohta* is a low signal such that LED would not be powered or on. Thus the references either in singular or in combination teach the above claim limitation(s).

As to **claim 15**, see similar rejection for claim 2 with respect to a LED as a display.

Allowable Subject Matter

6. **Claim 13** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Derrick W. Ferris whose telephone number is (571) 272-3123. The examiner can normally be reached on M-F 9 A.M. - 4:30 P.M. E.S.T.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau Nguyen can be reached on (571) 272-3126. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Derrick W. Ferris
Examiner
Art Unit 2663

DWF

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SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600 9/2/04